CLAIMS:

1. Apparatus for controlling a processor in a data processing system, comprising:

a first interface configured to receive a reset signal from said data processing system;

a second interface coupled to a halt terminal of said processor;

a third interface configured to receive a release signal; and

a controller configured to halt said processor in response to said reset signal and release said processor from a halt condition in response to said release signal.

2. The apparatus of claim 1, wherein said processor is embedded within an integrated circuit.

3. The apparatus of claim 2, wherein said first interface, said second interface, said third interface, and said controller are disposed within said integrated circuit.

4. The apparatus of claim 3, wherein said integrated circuit is a programmable logic device, and wherein said first interface, said second interface, said third interface, and said controller are defined by programmable logic of said programmable logic device.

5. The apparatus of claim 1, wherein said controller comprises a flip-flop having a set terminal configured to provide one of said first interface and said third interface, a clear terminal configured to provide the other of said first interface and said third interface, and an output terminal configured to provide said second interface.

6. The apparatus of claim 1, further comprising:

at least one additional interface configured to receive halt signals from said data processing system;

wherein said controller comprises:

a flip-flop having a set terminal configured to provide one of said first interface and said third interface, a clear terminal configured to provide the other of said first interface and said third interface, and a flip-flop output terminal; and

a logic gate coupled to said flip-flop output terminal and said at least one additional interface, said logic gate having a logic gate output terminal configured to provide said second interface.

7. Apparatus for initializing a data processing system having a processor, comprising:

a halt controller having a first interface configured to receive a reset signal from said data processing system, a second interface configured to drive a halt terminal of said processor with a halt signal in response to said reset signal, and a third interface; and

a control unit for generating a release signal to drive said third interface, said release signal operative to release said processor from a halt condition.

8. The apparatus of claim 7, wherein said control unit comprises a counter having a carry-out terminal coupled to said third interface.

9. The apparatus of claim 8, wherein said counter is configured to reset in response to said reset signal and provide said release signal via said carry-out terminal.

10. The apparatus of claim 7, wherein said processor is coupled to said third interface and said control unit is

coupled to a control interface of said processor, and wherein said control unit is configured to drive said control interface with control information, said control information operative to cause said processor to drive said third interface with said release signal.

11. The apparatus of claim 7, wherein said processor is embedded within an integrated circuit, and wherein said halt controller is disposed within said integrated circuit.

12. The apparatus of claim 11, wherein said integrated circuit is a programmable logic device, and wherein said halt controller is defined by programmable logic of said programmable logic device.

13. A method of controlling a processor within a data processing system, comprising:

maintaining said processor in a halt condition in response to reset information from said data processing system;

configuring at least one memory resource in communication with said processor; and

releasing said processor from said halt condition.

14. The method of claim 13, wherein said configuring step comprises:

storing data in said at least one memory resource at a location associated with a reset vector of said processor.

15. The method of claim 14, wherein said data comprises code configured to be executed by said processor.

16. The method of claim 14, wherein said processor is released from said halt condition in response to storage of said data.

17. The method of claim 14, wherein said processor is released from said halt condition in response to elapse of a predefined time period.

18. The method of claim 13, wherein said processor is embedded within an integrated circuit, and wherein said reset information is generated in response to initialization of said integrated circuit.

19. A method of controlling a processor within a data processing system, comprising:

maintaining said processor in a halt condition in response to reset information from said data processing system;

stopping an execution cycle of said processor;

releasing said processor from said halt condition;

configuring at least one memory resource in communication with said processor; and

starting said execution cycle of said processor.

20. The method of claim 19, wherein said configuring step comprises:

storing data in said at least one memory resource at a location associated with a reset vector of said processor.

21. The method of claim 20, wherein said data comprises code configured to be executed by said processor.

22. The method of claim 20, wherein said processor is started in response to storage of said data.

23. The method of claim 19, wherein said configuring step comprises:

storing data in said at least one memory resource at a

location; and

setting a program counter of said processor to said location.

24. The method of claim 19, wherein said processor is embedded within an integrated circuit, and wherein said reset information is generated in response to initialization of said integrated circuit.